CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

QUANTUM WIRE GATE DEVICE AND METHOD OF MAKING SAME
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At page 2, line 1.

B3 BACKGROUND INFORMATION.

At page 2, line 6

B4 TECHNICAL FIELD.

At page 2, beginning at line 16.

A field effect transistor (FET) is a fundamental building block of integrated circuits. Where metal oxide semiconductor (MOS) devices are approaching the limits of scaling based upon known fundamental technique, optimization of different components has allowed the FET to continue in the process of miniaturization. The decrease in supply voltage, however, has caused acceptable performance in the 0.7X scaling to become increasingly elusive. What is needed is a method of achieving gate dimensions that overcome scaling limits of the prior art.

At page 3, beginning at line 2.

In order to understand the manner in which embodiments of the present invention are obtained, a more particular description of embodiments of the invention briefly described above will be rendered by reference to the appended drawings. Understanding that these drawings depict only typical embodiments of the invention that are not necessarily drawn to scale and are not therefore to be considered to be limiting of its scope, the embodiments of the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

At page 3, the paragraph beginning at line 9.

Figure 1a is an elevational cross-section fractional view that depicts preliminary fabrication of a first layer for a quantum wire, double gate device according to an embodiment;

At page 3, the paragraph beginning at line 21.

Figure 2a is an elevational cross-section view of a substrate with a patterned oxide disposed thereon that has been precisely spaced apart according to an embodiment;

At page 5, the paragraph beginning a line 1.

Figure 5 is an elevational cross-section fractional view of a quantum wire gate according to an embodiment;

At page 5, the paragraph beginning at line 3.

Figure 6 is an elevational cross-section fractional view of a quantum wire gate according to an embodiment;

At page 5, the paragraph beginning at line 5.

Figure 7 is an elevational cross-section fractional view of a quantum wire gate according to an embodiment;

At page 5, the paragraph beginning at line 7.

Figure 8 is an elevational cross-section fractional view of a quantum wire gate according to an embodiment;

At page 5, the paragraph beginning at line 9.

Figure 9 is an elevational perspective view of a quantum wire gate according to an embodiment;

At page 5, the paragraph beginning at line 10.

Figure 10 is a block diagram that illustrates a process flow according to an embodiment;

At page 6, the paragraph beginning a line 14, and ending a page 7, line 2.

Figure 1a is an elevational cross-section fractional view of a larger structure that depicts preliminary fabrication of a quantum wire, spacer double gate device, depicted herein by

reference numeral 10. Device 10 is fabricated by providing a substrate 12 and by patterning a first oxide 14 upon substrate 12. First oxide 14 has a characteristic width and a characteristic pitch. **Figure Ib** illustrates formation of a first nitride layer 16 over first oxide 14 and substrate 12. First nitride layer 16 has a thickness in a range from about 5 nm to about 20 nm, preferably about 10 nm. First nitride layer 16 may be deposited by chemical vapor deposition (CVD), by physical vapor deposition (PVD), by nitridation of a PVD or CVD metal layer, or by other known methods. One method of forming first nitride layer 16 is to directly form a nitride layer 16 upon substrate 12 and first oxide 14 by CVD or PVD ora nitride such as a metal nitride. Preferably, first nitride layer 16 is formed by CVD of a refractory metal nitride such as silicon nitride.

At page 7, the paragraph beginning at line 17 and ending on page 8, line 2.

Figure Ie illustrates further processing of structure 10. An anisotropic etch has been carried out on substrate 12 with the use of first nitride spacer mask 18. Etching into substrate12 is carried out under conditions that will allow the formation of a quantum wire 20. Quantum wire 20 has the property of having a width W, defined by the thickness of first nitride layer 16, that is smaller than the mean free path of electrons that flow therein under semiconductive conditions. Quantum wire 20 may be an integral part of substrate 12. Even though doping of substrate 12 and of quantum wire 20 may be identical, due to the multiple gate structure and/or the proximity of semiconductive channels in a double gate configuration, a semiconductive transaction occurs only in quantum wire 20. This phenomenon will be set forth below.

At page 8, the paragraph beginning at line 2.

Figure 1f illustrates further processing of structure 10 depicted in Figure 1e, wherein quantum wire 20 has been overlaid with a gate layer 22. Gate layer 22 is preferably a metal-like material such as heavily p- or n-doped (e.g. about 1 X $10^{20}/cm^3$) or undoped polycrystalline silicon. It may also be a metal. In a preferred embodiment gate layer 22 may be formed by CVD followed by planarization such as by chemical-mechanical polishing (CMP). In this embodiment, a plurality of channels includes a quantum wire 20 that forms a first semiconductive channel 20 that is spaced apart by a trench 32 from a second quantum wire 20 that forms a second semiconductive channel 20. The trench 32 has a width is greater than the channel width W,

preferably less than about five times the semiconductive channel width W.

At page 8, the paragraph beginning a line 17.

In accordance with an embodiment of the present invention, a method of forming a device with uniform and closely spaced quantum wires is provided. Figure 2a is an elevational cross-section view of a structure 200 that includes a substrate 12 with a patterned first oxide 14 disposed thereon. Patterned first oxide 14 is precisely spaced apart to allow crowding of quantum wires into a minimum area. In one embodiment, patterned first oxide 14 has a characteristic width, W, in a range from about 50 nm to about 200 nm, preferably about 100 nm. Patterned first oxide 14 has a characteristic pitch, P, in a range from about 150 nm to about 600 nm, preferably about 300 nm. Thus, where W is equal to a given width X, P is equal to a pitch 3X.

At page 10, the paragraph beginning at line7.

Figure 2i illustrates further processing, wherein quantum wires 20 have been formed by etching into substrate 12. Where the characteristic channel width, W, was about 100 nm and the characteristic pitch, P, was about 300 nm, structure 10 has a plurality of quantum wires 20 that have a channel width 30 of about 10 nm. Additionally, quantum wires 20 are uniformly spaced apart by a trench 32 that has a trench width 34 of about 20 nm. Hence, where quantum wire 20 is about 10 nm, or "X", trench 34 is about 20 nm or "2X".

At page 10, the paragraphs beginning at line 17 and ending on page 12, line 4.

Other dimensions of quantum wire 20 and of second nitride spacer mask 28 include the quantum wire height 36 and the second nitride spacer mask height 38. Preferably, quantum wire 20 is at least square in cross-sectional shape. Optionally, quantum wire 20 may have an aspect ratio of height 36-to-channel-width 30 in a range from about 1.1 to about 5. Second nitride spacer mask 28 may be of any aspect ratio that is suited or incidental to a preferred fabrication scheme. Examples of the aspect ratio range of the second nitride spacer mask 28 include from about 0.2 to about 10. Preferably, second nitride spacer mask 28 has an aspect ratio of about 1 or greater. Structure 200 depicted in Figure 2i may be further processed as set forth herein to form a quantum wire gate device.

Another uniform spacing scheme may be accomplished according to an embodiment of the

present invention as illustrated in **Figure 3a**. In this embodiment, a structure such as second nitride spacer mask 28 is overlaid with a material such as an oxide layer 82. In **Figure 3b**, oxide layer 82 has been planarized back to about the top of second nitride spacer mask 28 to form an oxide block 84. With oxide block 84 in place, a directional etch may be carried out to create a quantum wire 320 and a trench 32 that spaces apart two quantum wires 320. By conducting the inventive method of this embodiment similar to the inventive method depicted in Figures 2, trench 32 has a width that is less than the quantum wire channel width.

Figure 4 is an elevational cross-section fractional view of an inventive quantum wire double gate 400. A double-gate quantum wire 420 comprises two semiconductive channels 42, 44 that are depicted by estimation phantom lines to delineate semiconductive transaction areas. As a whole, double-gate quantum wire 420 may be considered a semiconductive channel comprising a channel length and a channel width W. The channel length is orthogonal to the plane of the Figure. A dielectric layer such as a gate oxide layer 40 may be formed upon the semiconductive channel length as well as upon substrate 12. After formation of a first nitride spacer mask 18, and the etching of the double-gate quantum wire 420, a gate layer 422 is disposed over the double-gate quantum wire 420.

Figure 5 is an elevational cross-section fractional view of an inventive quantum wire triple gate 500. A triple-gate quantum wire 520 comprises three semiconductive channels 42, 44, and 46 that are depicted by estimation with phantom lines to delineate semiconductive transaction areas. As a whole, triple-gate quantum wire 520 may be considered a semiconductive channel comprising a channel length and a channel width W. The channel length is orthogonal to the plane of the Figure. A dielectric layer such as a gate oxide layer 40 may be formed upon the semiconductive channel length and channel width as well as upon substrate 12. Quantum wire triple gate 500 comprises three semiconductive channels 42, 44, and 46. A gate layer 522 is disposed over the double-gate quantum wire 520.

At page 13, the paragraph beginning at line 8.

Figure 7 illustrates an SOI structure 700 that includes an insulator substrate 50 that forms the SOI precursor set upon silicon 52. Therefrom, quantum wires 720 have been formed beneath a spacer mask such as second nitride spacer mask 28. In this embodiment, quantum wire 720 has been totally isolated from other electrically conductive or semiconductive material. A dielectric

layer such as a gate oxide layer 40 may be formed upon the semicondutive channel length. A gate layer 722 is disposed over the double-gate quantum wire 720 and fills the trench 32. It is understood that the SOI scheme may be applied in any of the embodiments set forth herein.

At page 14, the paragraphs beginning at line 1 and ending on page 15, line 8.

It now become apparent that combination of an SOI with a self-aligned doping region may be carried out. In this embodiment, an SOI quantum wire is constructed that does not achieve complete isolation of the wires from their silicon substrate. In other words, etching does not proceed to the extent that the etch stops on the insulator; it stops short of this etch depth. Isolation is approximated, however, by the implantation of a doping region as set forth above. The doping region may extend to the insulator substrate, or it may only extend to a depth that causes the quantum wires to be effectively isolated from their monocrystalline silicon substrate. In this embodiment, the plurality of quantum wires maintains a structural integrity with their monocrystalline silicon substrate, but they are effectively isolated from each other as well as from the substrate. This embodiment may be achieved by forming a structure such as structure 800 as depicted in Figure 8, upon an insulator substrate such as insulator substrate 50, as depicted in Figure 7.

Figure 9 is an elevational perspective view of an inventive quantum wire gate structure 900. A quantum wire 920 is disposed upon an insulator substrate 50. Quantum wire 920 has been patterned with the use of a spacer mask such as second nitride spacer mask 28. A gate layer 922 is disposed over quantum wire 920 and second nitride spacer mask 28 to create a quantum wire double gate in this embodiment. A gate oxide (not pictured) is formed upon the length 56 of quantum wire 920. An insulator 58 may also be formed. Additionally, where quantum wire 920 is to connect with a contact in a contact corridor, a spacer gate is to be formed between a contact landing area 60 and gate layer 922 by the traditional method of nitride/oxide deposition and an RIE spacer etch.

Figure 10 is a process flow diagram that illustrates an inventive method embodiment of forming a quantum wire gate. The process 1000 begins at block 1010 with patterning a first oxide upon a substrate. At block 1020 the process continues by forming a first nitride spacer mask upon the first oxide. Next, a first oxide spacer mask is formed at block 1030. The first oxide spacer mask is formed upon the first nitride spacer mask. The process continues at block t 040 by forming a

second nitride spacer mask upon the first oxide spacer mask. At block 1050, a plurality of channels is formed in the substrate. The plurality of channels are aligned to the second nitride spacer mask. At block 1060, a gate layer is formed over the plurality of channels. According to the present invention, each of the plurality of channels is narrower than the mean free path of semiconductive electron flow therein.